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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

NOTIFICATION DATE	DELIVERY MODE
09/13/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/087,672	AASHEIM ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11,13-19,21-26,28-34 and 36-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11,13-19,21-26,28-34 and 36-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on July 27, 2007. Claims 9 and 16 are amended; and claims 45-52 are cancelled. Therefore, claims 1, 3-11, 13-19, 21-26, 28-34 and 36-44 are currently pending in this application.

2. The rejections of claims 9-11, 13-19 and 21-22 under 101 and 112 have been overcome by the amendment made in the last response.

3. Applicant's arguments filed on July 27, 2007 have been considered but they are not persuasive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5-11, 15-18, 22-25, 29-33 and 37-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban (USPN: 5,799,168) in view of Sinclair et al. (USPN: 6,725,321) hereinafter, Sinclair further in view of Blumenau (USPN: 5,875,478) and Hall (USPN: 6,253,281).

As per claim 1, Ban teaches that one or more computer-readable media (the combination of flash array and standardized flash controller in Fig. 1) comprising a flash memory driver (the standardized flash controller in Fig. 1; i.e. the group of

interfaces/controllers, between the CPU and the flash memory) that is executable by a computer to interface between a file system and one or more flash memory media, the flash memory driver comprising: flash abstraction logic (i.e. the group of interfaces/controllers, between the CPU and the flash memory) and invokable by the file system to manage flash memory operations without regard to the type of the one or more flash memory media (e.g. see Col. 2, lines 36-38); and flash media logic (a simple discrete logic or interface) configured to interact with different types of the flash memory media (any flash chip); wherein the flash abstraction logic invokes the flash media logic to perform memory operations (generic commands) that are potentially performed in different ways depending on the type of the flash memory media (e.g. see the abstract, Col. 2, lines 36-48; Col. 4, lines 33-39, 61-65 and claim 2). The further limitation of the flash memory driver is having flash memory medium agnostic is also taught by Ban, i.e. Ban also teaches that the flash memory driver, i.e. the whole group of interfaces/controllers, between the CPU and the flash memory (e.g. see Fig. 2). Therefore, even though a unique controller is being placed on each individual flash chip, "the group of interfaces/controller" as a whole manages flash memory operations without regard to the type of the one or more flash memory media as being claimed. Ban also teaches that the flash driver (the standardized flash controller in Fig. 1) is located remotely from the flash memory medium (i.e. the flash array in Fig. 1) (e.g. see Fig. 1).

However, Ban failed to teach that one of the flash memory operations includes performing wear-leveling operations associated with the flash memory medium by way

of circular and continuous advancement of a write pointer. Sinclair, on the other hand, teaches about performing the wear-level operation in the flash memory by using the cyclic write pointer and single sector write management (e.g. see Col. 13, lines 46-55). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teachings of Sinclair in the flash memory driver taught by Ban so the uniform wear leveling throughout the flash medium can be achieved.

Neither Ban nor Sinclair teaches the further limitation of having the flash memory driver residing as a component within the operating system of the computer system. Blumenau, however, teaches about storing the storage drivers as a component within the operating system (OS) (e.g. see Col. 3, lines 6-26). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to include the flash memory driver taught by the combination of Ban and Sinclair within the OS as taught by Blumenau. In doing so, the different flash memory drivers can be included as a part of the OS without installing additional hardware. Therefore, the cost of hardware relative to the software driver and the size of the system the portability are reduced. Furthermore, the software drivers can be modified/added from the remote location.

However, none of them clearly disclose that the flash media logic is programmable to permit users to match particular medium requirements of a specific manufacturer. Hall, on the other hand, teaches the flash media logic (i.e. the code in the microcontroller that contains particular subroutines which can be selected based on

the type of flash media) is programmable to permit users to match particular medium requirements of a specific manufacturer (e.g. see Col. 5, lines 41-48). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teachings of Hall in the flash memory driver taught by the combination of Ban, Sinclair and Blumenau. In doing so, the end user can get the flexibility of customizing the flash memory driver by programming the flash media logic suitable for the specific manufacturer of the flash media. Therefore, it is being advantageous.

As per claims 5 and 6, the combination of Ban, Sinclair, Blumenau and Hall teaches the claimed invention as described above and furthermore, Ban teaches the flash memory driver, wherein one of the flash memory operations includes mapping status information associated with physical sectors of the flash memory medium for use by the file system, i.e. translating commands from/to physical sectors of the flash memory medium to/from commands for used in the file system (CPU) (e.g. see Col. 5, lines 29-37).

As per claim 7, the combination of Ban, Sinclair, Blumenau and Hall teaches the claimed invention as described above and furthermore, Ban teaches the flash memory driver, wherein the flash medium logic (simple discrete logic) is a user programmable to read, write and erase data to and from the flash memory medium (e.g. see Col. 3, line 49 – Col. 4, line 13).

As per claim 8, the combination of Ban, Sinclair, Blumenau and Hall teaches the claimed invention as described above and furthermore, Sinclair teaches that the flash

media logic (i.e. the controller chip 8 in Fig. 2) is configured to perform the error code correction (ECC) associated with the flash memory media (e.g. see Col. 11, lines 3-7 and Fig. 2).

As per claim 16, see argument with respect to the rejection of claims 1 and 7. Claim 16 is rejected based on the same rationale as the rejection of claims 1 and 7.

As per claim 17, the combination of Ban, Sinclair, Blumenau and Hall teaches the claimed invention as described above and furthermore, Ban teaches that the flash abstraction logic that is interface/controller, between the CPU and the flash memory, passes specific commands associated with certain types of flash memory media directly to the flash medium logic (a simple discrete logic or interface) for translation and further execution (e.g. see Col. 2, lines 36-48 and Fig. 1).

As per claims 23 and 29, the combination of Ban and Sinclair teaches a processing device that uses a flash memory medium for storage of data, comprising: a file system (the flash file system), configured to control data storage for the processing device (i.e. the CPU in Fig. 1) (e.g. see Col. 2, lines 17-23); flash media logic (a simple discrete logic or interface which comprises the command register) configured to perform physical sector operations to a flash memory medium based on physical sector commands, wherein the flash medium logic comprises a set of programmable entry points that can be implemented by a user to interface with the type of flash memory medium selected (e.g. see Col. 3, lines 15-24); and flash abstraction logic that is interface/controller, between the CPU and the flash memory, configured to maintain flash memory requirements, which are common to a plurality of different flash memory

media, that are necessary to operate the flash memory medium (e.g. see Col. 2, lines 36-48 and Fig. 1).

Neither Ban nor Sinclair teaches the further limitation of having the flash memory driver residing as a component within the operating system of the computer system. Blumenau, however, teaches about storing the storage drivers as a component within the operating system (OS) (e.g. see Col. 3, lines 6-26). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to include the flash memory driver taught by the combination of Ban and Sinclair within the OS as taught by Blumenau. In doing so, the different flash memory drivers can be included as a part of the OS without installing additional hardware. Therefore, the cost of hardware relative to the software driver and the size of the system the portability are reduced. Furthermore, the software drivers can be modified/added from the remote location.

However, none of them clearly disclose that the flash media logic is programmable to permit users to match particular medium requirements of a specific manufacturer. Hall, on the other hand, teaches the flash media logic (i.e. the code in the microcontroller that contains particular subroutines which can be selected based on the type of flash media) is programmable to permit users to match particular medium requirements of a specific manufacturer (e.g. see Col. 5, lines 41-48). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teachings of Hall in the flash memory driver taught by the combination of Ban, Sinclair and Blumenau. In doing so, the end user can

get the flexibility of customizing the flash memory driver by programming the flash media logic suitable for the specific manufacturer of the flash media. Therefore, it is being advantageous.

As per claim 24, see argument with respect to the rejection of claim 17. Claim 24 is rejected based on the same rationale as the rejection of claim 17.

As per claim 33, see argument with respect to the rejection of claims 16 and 17. Claim 33 is rejected based on the same rationale as the rejection of claims 16 and 17.

As per claim 40, the combination of Ban, Sinclair, Blumenau and Hall teaches the claimed invention as described above and furthermore, Ban teaches that the method further comprises receiving read and write commands from a file system that is inherently embedded in the controller taught by Ban (e.g. see Col. 1, lines 35-39 and Col. 2, lines 40-44).

As per claim 41, the combination of Ban, Sinclair, Blumenau and Hall teaches the claimed invention as described above and furthermore, Ban teaches that one or more computer-readable media (the combination of flash array and standardized flash controller in Fig. 1) comprising computer-executable instructions (commands stored in the command register) that, when executed, perform the method as taught by Ban (e.g. see Col. 3, lines 15-24 and Fig. 1).

As per claims 15, 30 and 38, the combination of Ban, Sinclair, Blumenau and Hall teaches the claimed invention as described above and furthermore, Hall teaches the claimed invention as described above and furthermore, Hall teaches about issuing a set of programmable entry points that can be selected by an user to perform one or

more operations (i.e. particular subroutines which can be selected by the user to perform operations based on the type of flash media) (e.g. see Col. 5, lines 41-48). However, Hall does not clearly disclose about performing the error code correction (ECC) associated with the flash memory media. Sinclair teaches that the flash media logic (i.e. the controller chip 8 in Fig. 2) is configured to perform the error code correction (ECC) associated with the flash memory media (e.g. see Col. 11, lines 3-7 and Fig. 2).

As per claims 9, 18, 25 and 42-43, see argument with respect to the rejection of claim 1. Claims 9, 18, 25 and 42-43 are rejected based on the same rationale as the rejection of claim 1.

As per claims 11, 31 and 37, see argument with respect to the rejection of claim 6. Claims 11, 31 and 37 are rejected based on the same rationale as the rejection of claim 6.

As per claims 10, 22, 32, 39 and 44, see argument with respect to the rejection of claim 7. Claims 10, 22, 32, 39 and 44 are rejected based on the same rationale as the rejection of claim 7.

5. Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban in view of Sinclair and in view of Blumenau, Hall and Martwick (USPN: 6,493,807).

As per claims 3 and 4, the combination of Ban, Sinclair, Hall and Blumenau teaches the claimed invention as described above. However, none of Ban, Sinclair,

hall and Blumenau teaches that one of the flash memory operations includes maintaining data integrity of the flash memory medium and handling recovery of data associated with the flash memory medium after a power-failure. Martwick, on the other hand, teaches the method for updating the flash blocks so the data integrity gets maintained and the data can be recovered upon a power failure (e.g. see Col. 3, lines 37-39). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the method of updating the flash blocks as taught by Martwick in the flash memory driver taught by the combination of Ban, Sinclair, Hall and Blumenau to recognize the benefits as stated above.

Claims 13-14, 19, 21, 26, 28, 34 and 36 are rejected based on the same rationale as the rejection of claims 3 and 4.

6. Claims 1, 5-11, 15-18, 22-25, 29-33 and 37-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban in view of Sinclair, in view of Hall (USPN: 6,253,281) and further in view of Blumenau.

As per claim 1, Ban teaches that one or more computer-readable media (the combination of flash array and standardized flash controller in Fig. 1) comprising a flash memory driver (the standardized flash controller in Fig. 1) that is executable by a computer to interface between a file system and one or more flash memory media, the flash memory driver comprising: flash abstraction logic (i.e. the group of interfaces/controllers, between the CPU and the flash memory) that is invokable by the file system to manage flash memory operations (e.g. see Col. 2, lines 36-38); and flash

media logic (a simple discrete logic or interface); wherein the flash abstraction logic invokes the flash media logic to perform memory operations (generic commands (e.g. see the abstract, Col. 2, lines 36-48; Col. 4, lines 33-39, 61-65 and claim 2). However, Ban failed to teach that one of the flash memory operations includes performing wear-leveling operations associated with the flash memory medium by way of circular and continuous advancement of a write pointer. Sinclair, on the other hand, teaches about performing the wear-level operation in the flash memory by using the cyclic write pointer and single sector write management (e.g. see Col. 13, lines 46-55). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teachings of Sinclair in the flash memory driver taught by Ban so the uniform wear leveling throughout the flash medium can be achieved.

Although Examiner is totally disagree but just for the sake of argument, even if Ban fails to teach (a) the flash abstraction logic manages flash memory operations without regard to the type of the one or more flash memory media; (b) the flash media logic configured to interact with different types of the flash memory media; and (c) the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media, Hall teaches these limitations. Hall teaches that the flash abstraction logic (i.e. the code in the system controller 1 in Fig. 1) manages flash memory operations without regard to the type of the one or more flash memory media (i.e. 22 in Fig. 1), i.e. the flash memory driver is flash memory medium agnostic. Furthermore, Hall teaches the

flash media logic (i.e. the system controller 1 in Fig. 1) that is configured to interact with different types of the flash memory media; and the flash abstraction logic invokes the flash media logic to perform memory operations that are potentially performed in different ways depending on the type of the flash memory media (e.g. see Col. 5, lines 31-48). Hall also teaches that the flash driver (i.e. the code in the system controller 1 in Fig. 1) is located remotely from the flash memory medium (i.e. 22 in Fig. 1) (e.g. see Fig. 1). Hall also teaches that the flash media logic (i.e. the code in the microcontroller that contains particular subroutines which can be selected based on the type of flash media) is programmable to permit users to match particular medium requirements of a specific manufacturer (e.g. see Col. 5, lines 41-48). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teachings of Hall in the flash memory driver taught by the combination of Ban and Sinclair. In doing so, it will be appreciated by those skilled in the art that FLASH memories produced by different manufacturers require different operations to erase and/or write data to them and these sequences are stored for a number of different memories within the microcontroller ROM. Thus the disc drive manufacturer is not confined to a single FLASH memory type and the micro controller does not have to be reprogrammed if a different type of FLASH memory is used.

None of Ban, Sinclair and Hall teaches the further limitation of having the flash memory driver residing as a component within the operating system of the computer system. Blumenau, however, teaches about storing the storage drivers as a component within the operating system (OS) (e.g. see Col. 3, lines 6-26). Accordingly, it would

have been obvious to one of ordinary skill in the art at the time of the current invention was made to include the flash memory driver taught by the combination of Ban, Sinclair and Hall within the OS as taught by Blumenau. In doing so, the different flash memory drivers can be included as a part of the OS without installing additional hardware. Therefore, the cost of hardware relative to the software driver and the size of the system the portability are reduced. Furthermore, the software drivers can be modified/added from the remote location.

As per claims 5 and 6, the combination of Ban, Sinclair, Hall and Blumenau teaches the claimed invention as described above and furthermore, Ban teaches the flash memory driver, wherein one of the flash memory operations includes mapping status information associated with physical sectors of the flash memory medium for use by the file system, i.e. translating commands from/to physical sectors of the flash memory medium to/from commands for used in the file system (CPU) (e.g. see Col. 5, lines 29-37).

As per claim 7, the combination of Ban, Sinclair, Hall and Blumenau teaches the claimed invention as described above and furthermore, Ban teaches the flash memory driver, wherein the flash medium logic (simple discrete logic) is a user programmable to read, write and erase data to and from the flash memory medium (e.g. see Col. 3, line 49 – Col. 4, line 13).

As per claim 8, the combination of Ban, Sinclair, Hall and Blumenau teaches the claimed invention as described above and furthermore, Sinclair teaches that the flash media logic (i.e. the controller chip 8 in Fig. 2) is configured to perform the error code

correction (ECC) associated with the flash memory media (e.g. see Col. 11, lines 3-7 and Fig. 2).

As per claim 17, the combination of Ban, Sinclair, Hall and Blumenau teaches the claimed invention as described above and furthermore, Ban teaches that the flash abstraction logic that is interface/controller, between the CPU and the flash memory, passes specific commands associated with certain types of flash memory media directly to the flash medium logic (a simple discrete logic or interface) for translation and further execution (e.g. see Col. 2, lines 36-48 and Fig. 1).

As per claims 23 and 29, the combination of Ban, Sinclair and Hall teaches a processing device that uses a flash memory medium for storage of data, comprising: a file system (the flash file system), configured to control data storage for the processing device (i.e. the CPU in Fig. 1) (e.g. see Col. 2, lines 17-23); flash media logic (a simple discrete logic or interface which comprises the command register) configured to perform physical sector operations to a flash memory medium based on physical sector commands, wherein the flash medium logic comprises a set of programmable entry points that can be implemented by a user to interface with the type of flash memory medium selected (e.g. see Col. 3, lines 15-24); and flash abstraction logic that is interface/controller, between the CPU and the flash memory, configured to maintain flash memory requirements, which are common to a plurality of different flash memory media, that are necessary to operate the flash memory medium (e.g. see Col. 2, lines 36-48 and Fig. 1). Furthermore, Hall teaches that the flash media logic (i.e. the code in the microcontroller that contains particular subroutines which can be selected based on

the type of flash media) is programmable to permit users to match particular medium requirements of a specific manufacturer (e.g. see Col. 5, lines 41-48).

None of Ban, Sinclair and Hall teaches the further limitation of having the flash memory driver residing as a component within the operating system of the computer system. Blumenau, however, teaches about storing the storage drivers as a component within the operating system (OS) (e.g. see Col. 3, lines 6-26). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to include the flash memory driver taught by the combination of Ban, Sinclair and Hall within the OS as taught by Blumenau. In doing so, the different flash memory drivers can be included as a part of the OS without installing additional hardware. Therefore, the cost of hardware relative to the software driver and the size of the system the portability are reduced. Furthermore, the software drivers can be modified/added from the remote location.

As per claim 40, the combination of Ban, Sinclair, Hall and Blumenau teaches the claimed invention as described above and furthermore, Ban teaches that the method further comprises receiving read and write commands from a file system that is inherently embedded in the controller taught by Ban (e.g. see Col. 1, lines 35-39 and Col. 2, lines 40-44).

As per claim 41, the combination of Ban, Sinclair, Hall and Blumenau teaches the claimed invention as described above and furthermore, Ban teaches that one or more computer-readable media (the combination of flash array and standardized flash controller in Fig. 1) comprising computer-executable instructions (commands stored in

the command register) that, when executed, perform the method as taught by Ban (e.g. see Col. 3, lines 15-24 and Fig. 1).

As per claims 15, 30 and 38, the combination of Ban, Sinclair, Blumenau and Hall teaches the claimed invention as described above and furthermore, Hall teaches the claimed invention as described above and furthermore, Hall teaches about issuing a set of programmable entry points that can be selected by an user to perform one or more operations (i.e. particular subroutines which can be selected by the user to perform operations based on the type of flash media) (e.g. see Col. 5, lines 41-48). However, Hall does not clearly disclose about performing the error code correction (ECC) associated with the flash memory media. Sinclair teaches that the flash media logic (i.e. the controller chip 8 in Fig. 2) is configured to perform the error code correction (ECC) associated with the flash memory media (e.g. see Col. 11, lines 3-7 and Fig. 2).

As per claims 9, 18, 25 and 42-43, see argument with respect to the rejection of claim 1. Claims 9, 18, 25 and 42-43 are rejected based on the same rationale as the rejection of claim 1.

As per claims 11, 31 and 37, see argument with respect to the rejection of claim 6. Claims 11, 31 and 37 are rejected based on the same rationale as the rejection of claim 6.

As per claims 10, 22, 32, 39 and 44, see argument with respect to the rejection of claim 7. Claims 10, 22, 32, 39 and 44 are rejected based on the same rationale as the rejection of claim 7.

As per claim 16, see argument with respect to the rejection of claims 1 and 7. Claim 16 is rejected based on the same rationale as the rejection of claims 1 and 7.

As per claim 24, see argument with respect to the rejection of claim 17. Claim 24 is rejected based on the same rationale as the rejection of claim 17.

As per claim 33, see argument with respect to the rejection of claims 16 and 17. Claim 33 is rejected based on the same rationale as the rejection of claims 16 and 17.

7. Claims 3-4, 13-14, 19, 21, 26, 28, 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban in view of Sinclair, further in view of Hall, further in view of Blumenau and further in view of Martwick (USPN: 6,493,807).

As per claims 3 and 4, the combination of Ban, Sinclair, Hall and Blumenau teaches the claimed invention as described above. However, none of Ban, Sinclair, Blumenau and Hall teaches that one of the flash memory operations includes maintaining data integrity of the flash memory medium and handling recovery of data associated with the flash memory medium after a power-failure. Martwick, on the other hand, teaches the method for updating the flash blocks so the data integrity gets maintained and the data can be recovered upon a power failure (e.g. see Col. 3, lines 37-39). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the method of updating the flash blocks as taught by Martwick in the flash memory driver taught by the combination of Ban, Sinclair, Blumenau and Hall to recognize the benefits as stated above.

Claims 13-14, 19, 21, 26, 28, 34 and 36 are rejected based on the same rationale as the rejection of claims 3 and 4.

Remarks

8. As to the remark, Applicant asserted that, during the telephone interview, Examiner and Applicant agreed that making the combination of Ban and Blumenau references, as suggested by office, would run contrary to Ban's teachings of including, on each flash unit, its own unique controller. Therefore, the combination of Ban and Blumenau references is improper.

Examiner respectfully traverses Applicant's remark for the following reasons:

First of all, Examiner never agreed with Applicant during the interview as recited in the remarks submitted by applicant on 07/27/2007. Examiner simply suggested Applicant's representative to submit the arguments in the next official response as recited in the Interview Summary electronically submitted Applicant on 07/11/2007.

Examiner also would like to point out to Applicant that the 103 rejection(s) over Ban in view of Blumenau (and other references as recited in the rejection above) is proper. The Blumenau reference is merely introduced/used to teach and implement the feature of residing the flash memory driver as a component within the OS of the computer system. The whole reason to make the 103 (i.e. introduce two references) for this limitation is that the Ban does not teach this limitation/feature and the Blumenau does. If the Blumenau reference did not need to be introduced/used for this rejection(s),

then said limitation/feature would have been anticipated by and not obvious over the Ban reference.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Ishi et al. (USPN: 5,867,428) teaches about combining the memory driver into the OS (e.g. see Col. 17, lines 52-59)
- Krithivas et al. (USPN: 6,067,628) also teaches about including the filter driver, USB drivers and USB hub driver in the operating system (e.g. see Col. 4, lines 38-42)
- Mills et al. (USPN: 5,696,917) discloses programmable controller which can be programmed on a bank-by-bank basis based on the flash media type (e.g. see Col. 25, lines 13-22)
- Fandrich (USPN: 5,509,134) teaches about permitting users to match particular medium requirements of a specific manufacturer by programming the flash media logic (i.e. by customizing the algorithms stored in the program memory by programming the program memory for the controller 50 in Fig. 2) (e.g. see the abstract and Fig. 2)

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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